Device cost reduction

Qi Gao ---**Texas Instruments**

2015-03-28

Device cost

- Device cost
  - Wafer cost
  - Assembly cost
  - Test cost

- Device cost Reduction

  Reduce the cost of device while still keeping the same performance and the same quality

专业IC测试网
www.ictest8.com

Device cost reduction

- Wafer cost reduction
  - 200mm to 300mm.
  - Scribe line shrink → 80um to 60um.
  - Technology shrink → 0.18um to 0.16um.
  - …………
- Assembly cost reduction
  - Au to Cu wire conversion.
  - Etch leadframe to stamp leadframe conversion
  - Low cost Bom change
  - …………

专业IC测试网
www.ictest8.com

Device cost reduction

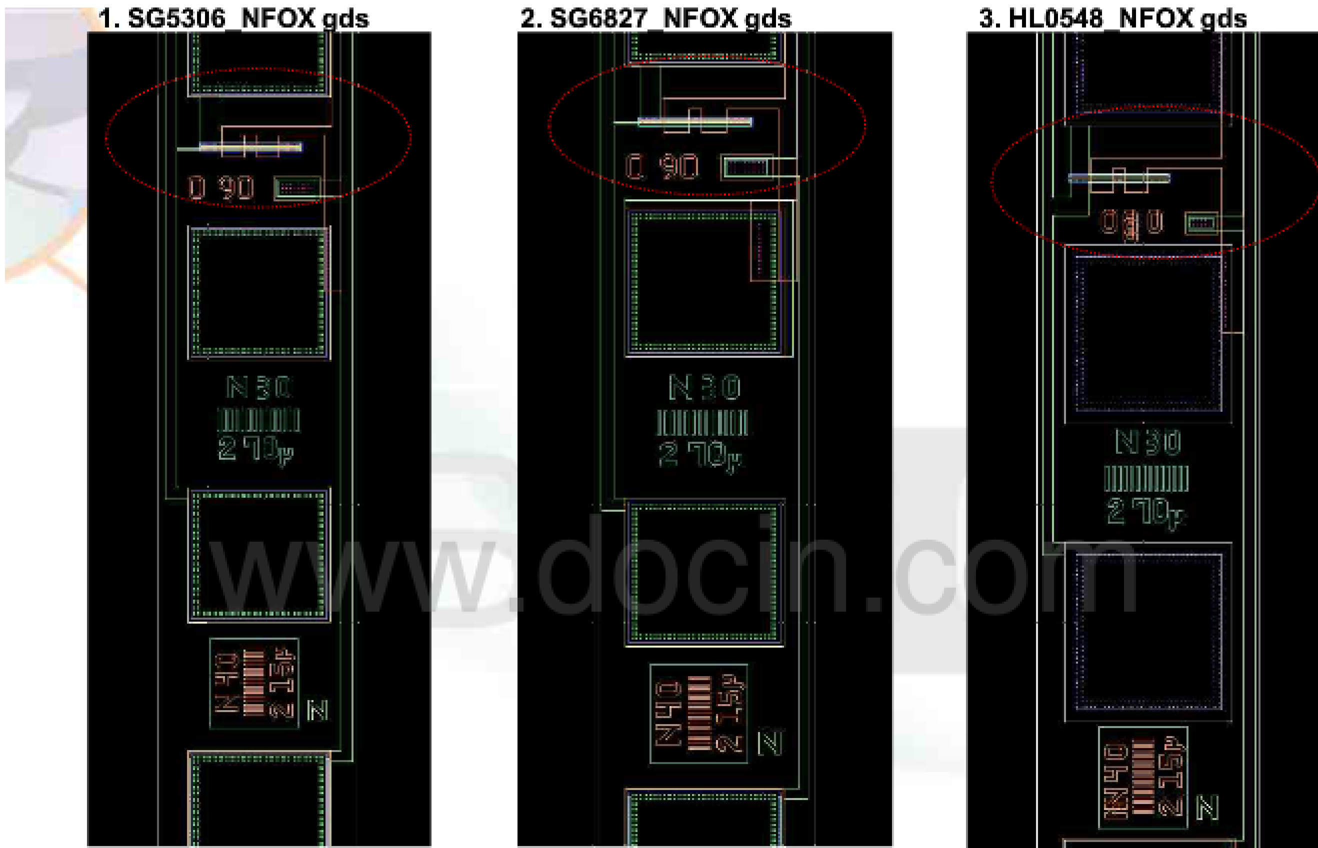
- Test cost reduction
  - TTR.
  - Full probe to sampling probe
  - Test platform conversion.
  - Test insertion removal.
  - …………

专业IC测试网
www.ictest8.com

Device cost reduction-Wafer cost reduction

Scribe line shrink. 80um to 60um

1. PCM test key-> is the PCM ok for 80um ok for 60um as well?



www.docin.com

专业IC测试网
www.ictest8.com

Device cost reduction-Wafer cost reduction

Scribe line shrink. 80um to 60um

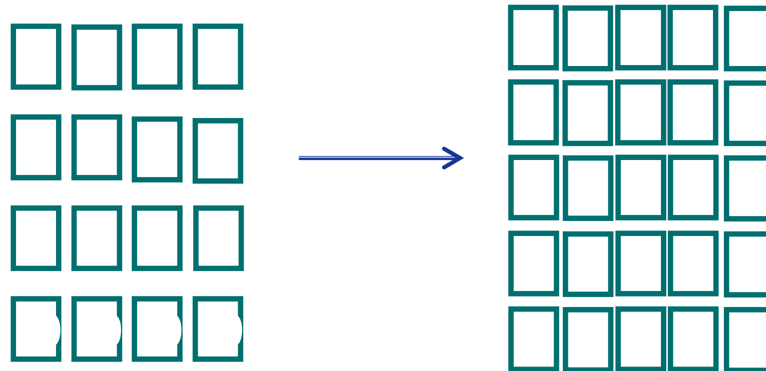
2. Assembly die saw process -> is the die saw process ok to support smaller scribe width?

专业IC测试网
www.ictest8.com

Device cost reduction-Wafer cost reduction

When we qualify to change the scribe width from 80 to 60 and release the new scribe to production.
What process will be changed?

1. Photo mask/ Photo process change



2. PCM card test/PCM card
3. Probe card/Probe test. (Probe card needs to rebuild if it is multi probe test)
4. Assembly die saw process

New mask set cost+New probe card cost+New PCM probe card
= (Wafer yielded cost/(Die per wafer)-Wafer yielded cost/(New die per wafer))*N

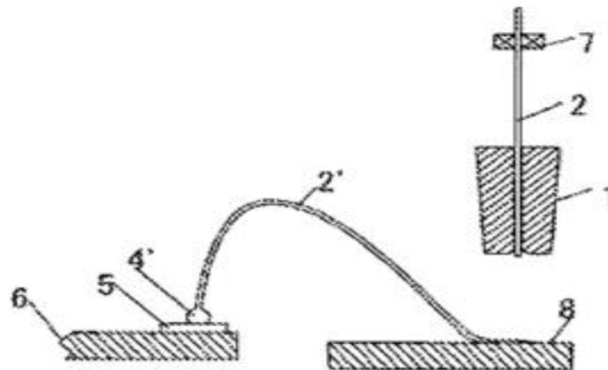
N -> the balance number that decides if it is cost effective to do the change

专业IC测试网
www.ictest8.com

Device cost reduction-Assembly cost reduction

Bonding wire material change ->Au wire to Cu wire change flow

1. Wafer structure study. Device current study.
   -> Bond pad material study. Bond pad size study
   -> wafer structure under the pad
   -> Current drive capability
2. Bonding wire DOE study→ find out the optimized ultrasonic force and frequency for each device

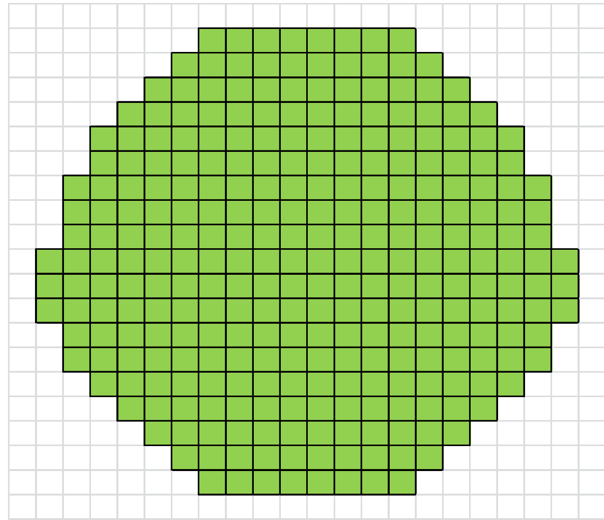


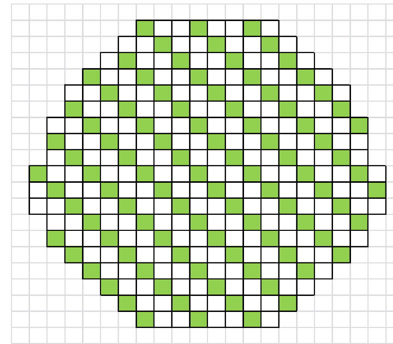
3. Qualification → HTSL/TC/AC….. It takes 3months to half a year to complete conversion

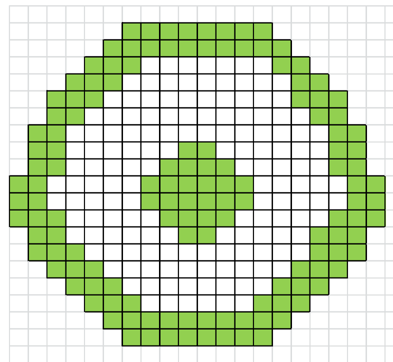
专业IC测试网
www.ictest8.com

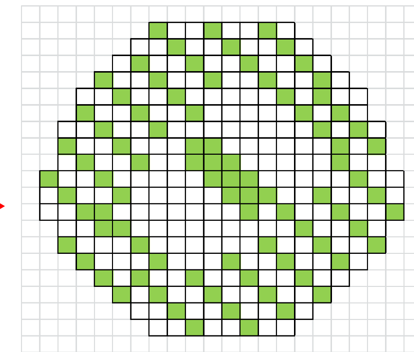
Device cost reduction-test cost reduction

❖Full probe to sampling probe









The sampling pattern can be randomly picked all over the wafer or can be picked based on the process defects.

What if it is a quad site test?

Not applicable for those devices with probe fuse, trim, ovst or mini burn-in

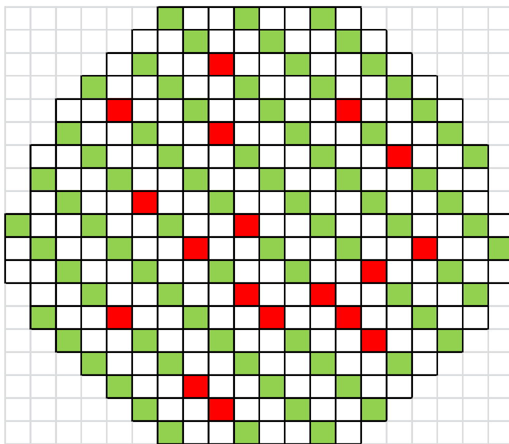
专业IC测试网
www.ictest8.com

Test cost reduction

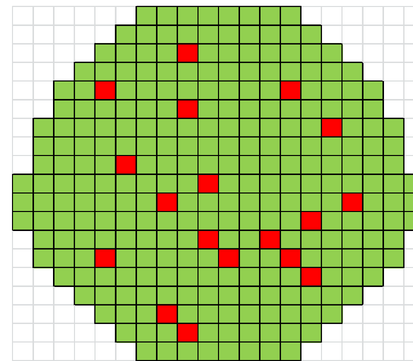
❖Probe cost

Full probe to sampling probe -> How to dispose when low yield happens

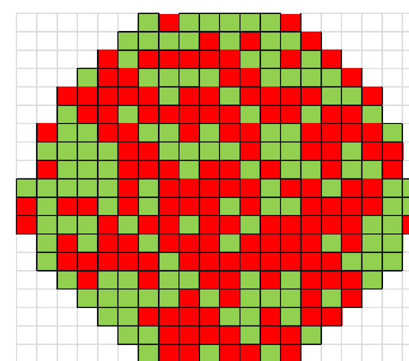
Suppose probe hold yield is 90%



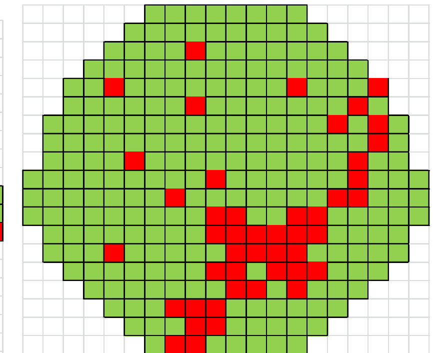
Sampling probe yield: 81%



Full probe yield: 94%



Need to scrap



Hold for process study

Turn on the full probe when the sample probe yield is less than the hold limit

Check the full probe yield and then dispose

专业IC测试网
www.ictest8.com

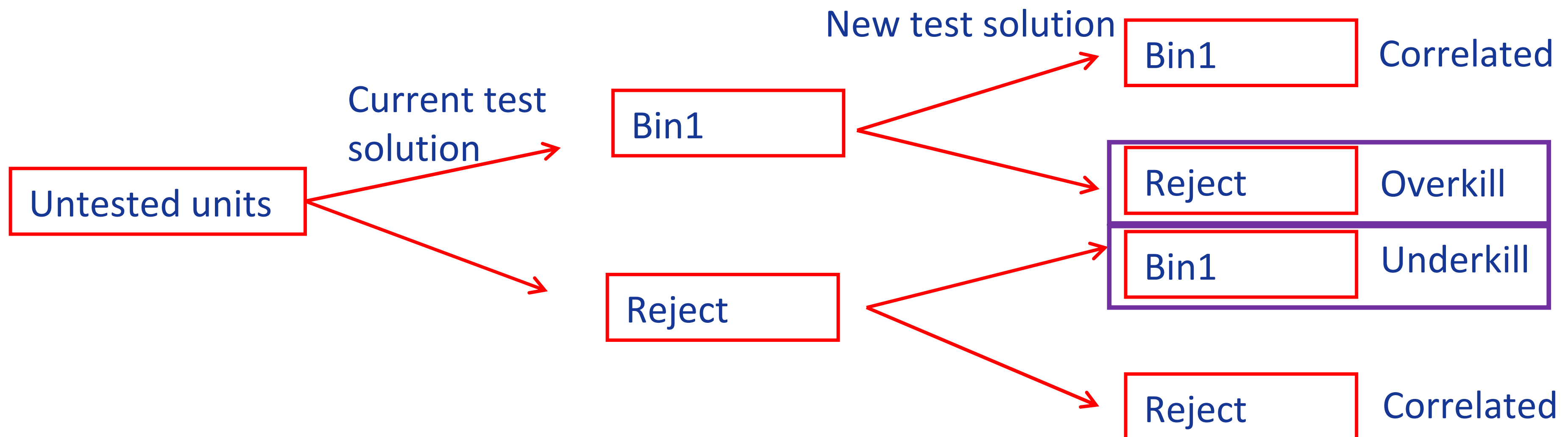
Test cost reduction

❖ Test platform conversion

Test platform conversion→ expand test site, reduce tester time, optimize test method

Assume the current test solution is ok

New test solution checkout flow



- Underkill is the unit group we need to study
- Overkill is the unit group that causes yield loss

专业IC测试网
www.ictest8.com

Q & A

专业IC测试网
www.ictest8.com

OVER

Thank You !

专业IC测试网
www.ictest8.com